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(71) Applicant (*for all designated States except US*): ASAT LIMITED [—/CN]; QPL Industrial Building, 138 Texaco Road, Tsuen Wan, NT Hong Kong (HK).

(71) Applicants and
(72) Inventors: MCLELLAN, Neil, Robert [US/CN]; #3 Tregunter Path Flat 3B, Mid Levels, Hong Kong (HK). PEDRON, Serafin, Jr. [US/US]; 2073 Solothurn Way, Manteca, CA 95337 (US). YEE, Lin, Tsui [—/CN]; Room 1510, Yiu Tung House, Tung Tau Estate, K/N, Hong Kong (HK).

(74) Agent: GASPAR, Christopher, J.; Milbank, Tweed, Hadley & McCloy, LLP, One Chase Manhattan Plaza, New York, NY 10005 (US).

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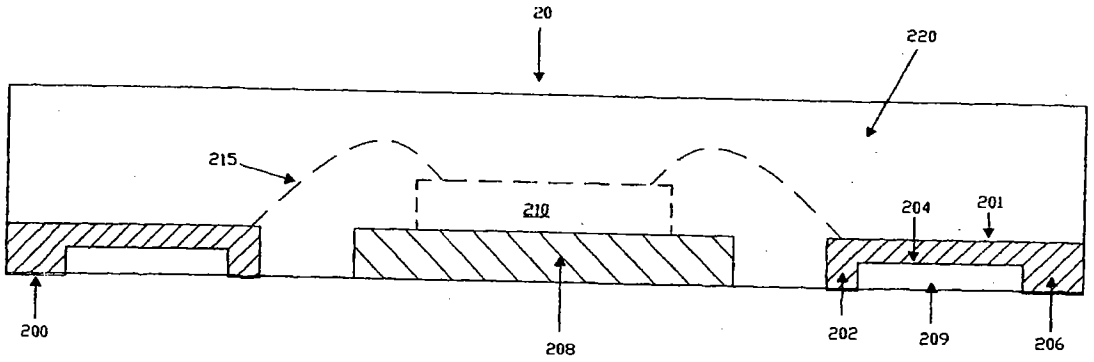
(54) Title: IMPROVED INTEGRATED CIRCUIT PACKAGE AND METHOD OF MANUFACTURING THE INTEGRATED CIRCUIT PACKAGE




(57) Abstract: The present invention relates to an integrated circuit package (10) and method of manufacturing an integrated circuit package (10). In one aspect, the present invention relates to an integrated circuit package (10) including a lead frame (100) having a lead (101) with an inner pad (102) and an outer pad(106) connected by a connection member (115); wherein a region of the inner pad 9102) and a region of the outer pad (106) are separated by a channel (109) extending through a width of the lead (101). Such an integrated circuit package (10) further includes a semiconductor die (110) electrically coupled with the inner pad (102) of the lead (101), and an encapsulant material (120) encapsulating at least a portion of said lead frame (101), wherein a portion of said outer pad (106) is exposed. In another aspect, the present invention relates to a method including providing a matrix of lead frames, each of the lead frames having a lead (101), forming a channel (109) extending through a width of the lead to create an inner pad (102), an outer pad (106) and a connection member (115) in the lead (101), electrically coupling a semiconductor die (110) with the inner pad (102), and encapsulating at least a portion of the lead frame (100) such that at least a portion of the outer pad (106) is exposed.

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# IMPROVED INTEGRATED CIRCUIT PACKAGE AND METHOD OF MANUFACTURING THE INTEGRATED CIRCUIT PACKAGE

## FIELD OF THE INVENTION

The present invention relates to integrated circuit packaging technology, and more particularly, to lead frames, integrated circuit packages, and methods of manufacturing such lead frames and packages.

## BACKGROUND OF THE INVENTION

A conventional lead frame may include a die attachment pad for accommodating a semiconductor die, as well as a number of leads connected to the semiconductor die. Such a conventional lead frame and semiconductor die may be packaged by being encapsulated within a plastic or resinous material. Various shapes and sizes of such packages exist. For example, U.S. Patent No. 6,229,200 to Mclellan, entitled "Saw-Singulated Leadless Plastic Chip Carrier," discloses a chip carrier having an encapsulation encapsulating a semiconductor die. In certain standard and conventional lead frames, the leads connected to the semiconductor die may be spaced somewhat far from the semiconductor die's bonding pads when the die is of a relatively small size compared to the lead frame. Therefore, in connection with certain packages, it may be advantageous to have a lead frame which includes a portion of a lead for attachment to the semiconductor die, and another portion of the lead for connection to an external device.

## SUMMARY OF THE INVENTION

In one aspect, the invention features an integrated circuit package including a lead frame with a lead having an inner pad and an outer pad connected by

a connection member, wherein a region of the inner pad and a region of the outer pad are separated by a channel extending through a width of the lead, a semiconductor die electrically coupled with the inner pad of the lead, and an encapsulant material encapsulating at least a portion of the lead frame, wherein a portion of the outer pad is exposed.

In another aspect, the invention features an integrated circuit package including a lead frame having a die attachment pad and a plurality of inwardly projecting leads, each of the leads having an inner pad and an outer pad, wherein a region of the inner pad and a region of the outer pad is separated by a channel extending through a width of the lead and connected by a connection member integral with the inner pad and the outer pad, the connection member having a thickness that is approximately half a thickness of the lead, a semiconductor die electrically coupled with the inner pad of the lead, and an encapsulant material encapsulating at least a portion of the lead frame, wherein a portion of the outer pad is exposed.

In yet another aspect, the invention features a method including providing a matrix of lead frames, each of the lead frames having a lead, forming a channel extending through a width of the lead to create an inner pad, an outer pad and a connection member in the lead, electrically coupling a semiconductor die with the inner pad, and encapsulating at least a portion of the lead frame such that at least a portion of the outer pad is exposed.

In a further aspect, the invention features a method including providing a lead frame having a lead, forming a channel extending through a width of the lead to create an inner pad, an outer pad and a connection member in the lead, electrically

coupling a semiconductor die with the inner pad, and encapsulating at least a portion of the lead frame such that at least a portion of the outer pad is exposed.

## BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing features, methods and other aspects of the invention are explained in the following description taken in connection with the accompanying drawings, wherein:

FIG. 1 shows a bottom view of an integrated circuit package 10 according to one embodiment of the present invention;

FIG. 2 is a simplified cross-sectional view, along line A-A, of the integrated circuit package 10 shown in FIG. 1;

FIG. 3 is a side view of the integrated circuit package 10 shown in FIG. 1;

FIG. 4 is a top view of a lead frame pre-assembly of the integrated circuit package 10 shown in FIG. 1;

FIG. 5 shows a bottom view of an integrated circuit package 20 according to another embodiment of the present invention;

FIG. 6 is a simplified cross-sectional view, along line B-B, of the integrated circuit package 20 shown in FIG. 5;

FIG. 7 is a top view of a lead frame pre-assembly of the integrated circuit package 20 shown in FIG. 5;

FIG. 8 shows a strip 800, including six sections 801-1 to 801-6, which may be used to make integrated circuit packages according to the present invention;

FIG. 9 shows a 3x3 array 900 of lead frames 100-1 to 100-9 which

may be provided in one or more of the sections 801-1 to 801-6 of the strip 800; and

FIGS. 10a – 10j show simplified cross-sectional views of certain steps of one type of process for making an integrated circuit package.

It is to be understood that the drawings are exemplary, and are not to be deemed limiting to the full scope of the appended claims.

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Various embodiments of devices according to the present invention will now be described with reference to the drawings.

FIG. 1 is a bottom view of an integrated circuit package 10 according to one embodiment of the present invention. Inner lead pads 102, outer lead pads 106 and a die attachment pad 108 of a lead frame 101 are shown exposed to the environment. Also shown is an encapsulant material 120 encapsulating certain internal portions of the integrated circuit package 10. The encapsulant 120 may be configured such that certain bottom surfaces of the die attachment pad 108 and the leads 101 are exposed.

In one embodiment, the lead frame 100 may have inner rows 105 of inner lead pads 102 arranged in a generally annular configuration, and outer rows 107 of outer lead pads 106 arranged in a generally annular configuration. The pitch between adjacent inner lead pads 102 and adjacent out lead pads 106 of a lead frame 100 of one embodiment may be different. As shown in the embodiment depicted in FIG. 1, the inner lead pads 102 of an inner row 105 of pads may be more closely spaced in relation to one another than the outer lead pads 106 of an outer row 107 of pads. Moreover, an inner lead pad 102 may have a smaller footprint or planform area

than a corresponding outer lead pad 106. In such an embodiment, the outer lead pads 106 may conform to a standard leadless plastic chip carrier configuration, while the inner lead pads 102 may be configured to more closely match the placement and spacing of bonding pads 112 of the semiconductor die 110.

The lead frame 100 may also include a die attachment pad 108 onto which a semiconductor die 110 may be attached. In such an embodiment, a soft solder may be used to attach the semiconductor die 110 to the die attachment pad 108, which may provide improved thermal performance.

Certain example dimensions are also depicted in FIG. 1. As shown in FIG. 1, each inner lead pad 102 may be smaller than its corresponding outer lead pad 106. In one embodiment, the width of a package 10 (shown as dimension "a") may be about 7.000 mm, the length of an outer lead pad 106 (shown as dimension "b") may be about 0.550 mm, each outer lead pad 106 may be about 0.230 mm wide (shown as dimension "c"), the pitch (shown as dimension "d") of adjacent outer lead pads 106 may be approximately 0.500 mm, and inner dimensions "e" and "f' may be about 4.300 mm.

FIG. 2 shows a cross-sectional view along line A-A of the integrated circuit package 10 shown in FIG. 1. This cross-sectional view shows certain components of the package 10 displayed in their respective positions relative to one another. One embodiment of an integrated circuit package 10 may generally include a lead frame 100, a semiconductor die 110 and an encapsulant 120.

The lead frame 100 of the integrated circuit package 10 of one embodiment may be made of an electrically conductive material such as, e.g., copper.

However, the lead frame 100 may be made of other metals, electrically conductive materials, or electrically conductive compounds in accordance with other embodiments of the present invention. The lead frame 100 may provide, at least in part, interconnections between the power, input and/or output terminals of the semiconductor die 110 and any external terminals that may be provided on the integrated circuit package 10. FIG. 2 shows a semiconductor die 110 connected to the inner lead pads 102 of the lead frame 100 via, for example, a gold thermo-sonic wire bonding technique. In such an embodiment, conductive gold wires 115 may interconnect bonding pads 112 formed on a top surface of the semiconductor die 110 to the leads 101 of the lead frame 100. Each such wire 115 may be bonded to both a bonding pad 112 of the semiconductor die 110 at one end, and the corresponding inner lead pad 102 at the other end. Each inner lead pad 102 may be connected to a corresponding outer lead pad 106 by an integrally formed connection portion 104 which, in one embodiment, may have a thickness dimension which is approximately half of the total thickness dimension "t" of a lead 101. A chemical etching process may be used to form a channel 109 in the lead 101 to create the connection portion 104 of a particular lead 101.

In one embodiment, portions of the upper and lower surfaces of a lead frame 100 may be plated 113 with solder or pure tin (Sn). This solder or pure tin plating 113 may provide an interface surface for mechanical, electrical or both types of connection of the integrated circuit package 10 to an external device (not shown). Alternatively, the lead frame 100 may be pre-plated with palladium to avoid silver migration.

As is further shown in FIG. 2, the semiconductor die 110 and lead frame 100 may be encapsulated in connection with an integrated circuit package 10 according to one embodiment of the present invention. The encapsulant 120 may be, for example, an epoxy based material applied by, for example, a liquid encapsulation process or a transfer molding encapsulation process. The top surface of the encapsulation may be given a distinctive pattern, which can be conferred to the encapsulation from the molding cavity during the molding process. This pattern, (e.g., a dimple array) may be used to orient the package 10 after singulation.

FIG. 3 is a side view of an example embodiment of an integrated circuit package 10 according to the present invention. As shown in FIG. 3, the external terminals of an integrated circuit package 10 may include an array of conductive members such as, e.g., solder balls 117. Such solder balls 117 may be attached to the outer lead pads 106 of the leads 101 using a reflow soldering process. In such an embodiment, the solder balls 117 function as electrical extensions of the leads 101, and may be capable of providing power, signal inputs and signal outputs to and from the semiconductor die 110. Such solder balls 117 may also provide clearance between the package 10 bottom and the printed circuit board (not shown) on which the package 10 is mounted. The solder balls 117 may be made of a variety of materials including lead (Pb) free solder. Such a configuration may be referred to as a type of ball grid array. Absent the solder balls 117, such a configuration may be referred to as a type of land grid array.

FIG. 4 depicts a top view of a lead frame 100 and semiconductor die 110 prior to encapsulation. As shown, a semiconductor die 110 is attached to the die

attachment pad 108 of the lead frame 100, and the bonding pads 112 of the semiconductor die 110 are connected via wires 115 to the inner lead pads 102 of the leads 101. The bonding pads 112 may provide locations at which the semiconductor die 110 may receive power and/or input signals, as well as transmit output signals. The wires 115 are one way to electrically couple a semiconductor die 110 of an integrated circuit package 10 to the leads 101 of the package 10 such that the semiconductor die 110 may receive power, input signals and/or output signals. The configuration of inner lead pads 102 as shown in FIG. 4 may allow the semiconductor die 110 to be connected to the lead frame 100 using a shorter length of wire 115 than may otherwise be required.

FIG. 5 shows a bottom view of an integrated circuit package 20 according to another embodiment of the present invention. In such an embodiment, the die attachment pad 208 may be shaped to accommodate the contours of inner lead pads 202 projecting inwardly from the periphery of the package 20.

FIG. 6 shows a cross-sectional view along line B-B of the integrated circuit package 20 shown in FIG. 5. The integrated circuit package 20 generally includes a lead frame 200, one or more semiconductor dies 210 and an encapsulant 220. FIG. 7 depicts a top view of a lead frame 200 and semiconductor dies 210-1, 210-2 prior to encapsulation. A number of semiconductor dies 210-1, 210-2 may be attached to the die attachment pad 208. The configuration of inner lead pads 202 as shown in FIG. 7 may allow two semiconductor dies 210-1, 210-2 to be connected to the lead frame 200 using a shorter length of wire 215 than may otherwise be required. Conductive wires 215 may be bonded between bonding pads 212 on each

semiconductor die 210-1, 210-2 and the inner lead pads 202 of the respective leads 201. In some cases, it may be desirable to position the inner lead pads 202 close to the semiconductor die 210. As shown, the connection portions 204 of certain leads 201 may be longer than others to allow certain inner lead pads 202 to be positioned more closely to bonding pads 212 of the semiconductor dies 210.

According to certain embodiments, shown in FIGS. 8 and 9, a lead frame 100, 200 may be formed in a matrix 900 of substantially identical lead frames. Furthermore, the matrix 900 of lead frames may be formed as one of multiple matrices of lead frames formed in a metal strip 800.

FIG. 8 shows a strip 800 including six sections 801-1 to 801-6 which may be used to fabricate integrated circuit packages 10, 20 of the embodiments described above. Using such a strip 800 may allow an assembly process to be carried out in automated assembly equipment and molds. Several lead frames 100, 200 may be produced in the form of, or otherwise assembled into, the strip 800 shown in FIG. 8 to accommodate semiconductor manufacturing equipment and process flows. Each of sections 801-1 to 801-6 may include a frame area 802 in which lead frames such as the lead frames 100, 200 described above may be formed using, for example, a chemical etching process, a stamping process, a combination of these processes and/or other processes. For example, an array of lead frames, may be formed in the frame area 802, as shown in FIG. 9. The periphery of the frame area 802 may contain alignment targets, tooling through-holes and other assembly features (labeled, collectively, by reference numerals 803a-803c) for use in automated assembly equipment.

As shown in FIG. 9, several lead frames may also be configured in a matrix array 900. For example, the strip 800 shown in FIG. 8 may contain six substantially identical sections 801-1 to 801-6, each of which may contain a 3x3 matrix array 900 similar to that shown in FIG. 9, which shows nine lead frames. A matrix array 900 like the one shown in FIG. 9 may be formed in the frame area 802 of each section 801 of the strip 800. Thus, in one configuration, fifty-four lead frames may be formed in each strip 800. Other configurations of either the strip 800, the matrix array 900, or both, may produce other volumes of lead frames. FIG. 9 shows lines 901, 902, 903, 904 along which the lead frame 100 may be cut to form integrated circuit packages.

Methods of manufacturing embodiments of integrated circuit packages will now be described with reference to the drawings, in particular, FIGS. 10a-10j.

A lead frame 100 may be formed into the configuration shown in the figures by a number of different processes including a chemical process (e.g., etching), a mechanical process (e.g., metal stamping), or a combination of these and/or other processes. As represented in FIGS. 10a-10b, in one aspect of one method embodiment according to the present invention, a lead frame 100 may be stamped from a sheet 1000 of copper to create a die attachment pad 108 and leads 101. In such an example method of manufacture, a lead frame 100 may be stamped while it is a part of a matrix array 900 of lead frames.

As depicted in FIG. 10c, after one or more lead frames 100 have been formed, an etching process may be used to etch a channel 109 into a bottom side of a lead 101 to create an inner lead pad 102, an outer lead pad 106 and a connection

portion 104. In one method embodiment, a chemical etching process may be used to create the channel 109. For example, a chemical etching process may include masking the bottom portion of the outer lead pad 106 and inner lead pad 102 such that material from the lead 101 is removed to form the channel 109. In one method embodiment, the etching process may remove material from the lead 101 to create a channel 109 that is approximately half the thickness of the lead 101.

In one example manufacturing process, as shown in FIG. 10d, a semiconductor die 110 may be attached to a die attachment pad 108 of the lead frame 100. A semiconductor die 110 may be mounted or attached to the die attachment pad 108 by epoxy or any suitable adhesive or fastening material. The semiconductor die 110 may also be attached using a soft solder to provide thermal conductivity between the semiconductor die 110 and the die attachment pad 108, thereby improving the thermal performance of the resulting package.

After the adhesive is cured, if required, the semiconductor die 110 may be wire-bonded to the inner lead pads 102 of the leads 101 using automated bonding equipment including a moving capillary device 1001 (see FIGS. 10e-10g). As shown in FIGS. 10e-10g, gold wires may be attached first to the bonding pads 112 of the semiconductor die 110 (FIG. 10e), and then to the inner lead pads 102 of the leads 101 (FIG. 10f) using automated bonding equipment with a flat plate support 1002.

Following attachment of the semiconductor die 110 to the lead frame 100, the pre-assembly may be encapsulated. As shown in FIG. 10h, a liquid encapsulation process or a transfer molding encapsulation process may be used to create packages 10, 20 such as those shown in FIGS. 1 - 7. Upon completion of this

assembly step of a particular assembly process, at least a portion of the outer lead pad 106 of the lead frame 100 may remain exposed to allow electrical connection to a printed circuit board (not shown), another semiconductor die and/or another integrated circuit package.

As shown in FIG. 10i, solder balls 117 may then be attached to the outer lead pads 106 of the leads 101 of each lead frame 100 using, for example, a reflow soldering process. Solder balls 117 attached to the exposed portions of the leads 101 may provide a clearance when the package 10, 20 is mounted on a printed circuit board. Such clearance may facilitate cleaning (e.g., cleaning of solder flux).

In one example method embodiment of the present invention, after the encapsulation and ball attachment assembly steps, the integrated circuit packages 10, 20 may be singulated into individual units using a saw singulation or punching technique (shown in FIG. 10j). During saw singulation, the strip 800 may be mounted to a wafer saw ring by an adhesive tape and saw-singulated using a conventional wafer saw. Singulation may be guided by alignment targets and other features (labeled as reference 901-904) formed, for example, on a lower surface of the strip 800 (for example, etched or stamped into the lead frame). Such targets or features may be incorporated into the strip 800 during its fabrication, and may help to maintain accurate size tolerances of each integrated circuit package produced in this way. In one example method, the underside of the strip 800 may face upward during a saw singulation process. Once singulated, an individual package 10, 20 may be ready for mounting onto a printed circuit board or other device. Optionally, the strip 800 then may be ink-marked or laser-marked and tin- or solder-plated to facilitate a subsequent

board-attachment step.

Although illustrative embodiments and example methods have been shown and described herein in detail, it is to be understood that there may be numerous variations, embodiments, and examples which may be equivalent to those explicitly shown and described. For example, the scope of the present invention may not necessarily be limited in all cases to execution of the aforementioned steps in the order discussed. Unless otherwise specifically stated, the terms and expressions have been used herein as terms and expressions of description, not of limitation. Accordingly, the invention is not to be limited by the specific illustrated and described embodiments and examples (or terms or expressions used to describe them), but only by the scope of the appended claims.

What is claimed is:

1. An integrated circuit package, comprising:

a lead frame comprising a lead comprising an inner pad and an outer pad connected by a connection member, wherein a region of said inner pad and a region of said outer pad are separated by a channel extending through a width of said lead;

a semiconductor die electrically coupled with said inner pad of said lead; and

an encapsulant material encapsulating at least a portion of said lead frame.

2. The integrated circuit package of claim 1, further comprising at least one wire attached between said semiconductor die and said inner pad.

3. The integrated circuit package of claim 2, wherein a length of said wire is about 150 mils or less.

4. The integrated circuit package of claim 1, wherein said connection member has a thickness that is approximately half a thickness of said lead.

5. The integrated circuit package of claim 1, wherein said connection member is integral with said inner pad.

6. The integrated circuit package of claim 5, wherein said connection member is integral with said outer pad.

7. The integrated circuit package of claim 1, wherein said lead is one of a plurality of inwardly projecting leads, each lead comprising an inner pad, and said inner pad of at least one of said leads projects further inward than another of said inner pads of said leads.

8. The integrated circuit package of claim 1, wherein said lead is one of a plurality of leads, each lead comprising an inner pad and an outer pad, and a distance between adjacent inner pads is less than a distance between adjacent outer pads.

9. The integrated circuit package of claim 1, further comprising a solder member attached to said exposed portion of said outer pad.

10. The integrated circuit package of claim 1, wherein said lead is one of a plurality of leads, each lead comprising an inner pad, and a width of at least one inner pad is less than a width of another inner pad.

11. The integrated circuit package of claim 1, wherein said encapsulant further encapsulates substantially all of said connection member.

12. The integrated circuit package of claim 1, further comprising a second semiconductor die electrically coupled with a second inner pad of a second lead.

13. The integrated circuit package of claim 1, wherein a thickness of said inner pad is substantially equal to a thickness of said outer pad.

14. An integrated circuit package, comprising:

a lead frame comprising a plurality of inwardly projecting leads, each of said leads comprising an inner pad and an outer pad, wherein a region of said inner pad and a region of said outer pad is separated by a channel extending through a width of said lead and connected by a connection member integral with said inner pad and said outer pad, said connection member having a thickness that is approximately half a thickness of said lead;

a semiconductor die electrically coupled with said inner pad of said lead; and

an encapsulant material encapsulating at least a portion of said lead frame.

15. A method, comprising:

providing a matrix of lead frames, each of said lead frames comprising a lead;

forming a channel extending through a width of said lead to create an inner pad, an outer pad and a connection member in said lead;

electrically coupling a semiconductor die with said inner pad; and

encapsulating at least a portion of said lead frame.

16. The method of claim 15, further comprising singulating said matrix to form a plurality of packages.

17. The method of claim 16, wherein said singulating comprises a saw singulation.

18. A method, comprising:

providing a lead frame comprising a lead;

forming a channel extending through a width of said lead to create an inner pad, an outer pad and a connection member in said lead;

electrically coupling a semiconductor die with said inner pad; and

encapsulating at least a portion of said lead frame.

19. The method of claim 18, wherein said forming comprises etching said channel into said lead.

20. The method of claim 19, wherein said etching comprises a chemical etching process.

21. The method of claim 19, wherein said etching comprises etching said channel to a thickness of approximately half a thickness of said lead.

22. The method of claim 18, further comprising attaching a solder member

to said outer pad.

23. The method of claim 18, wherein said electrically coupling comprises attaching a wire between said semiconductor die and said inner pad by a thermo-sonic bonding process.

24. The method of claim 23, wherein said bonding process comprises attaching said wire to a top side of said inner pad while a support contacts a bottom side of said inner pad and a bottom side of said outer pad.

25. The method of claim 23, wherein said support is a substantially flat plate.

26. A lead frame, comprising:

a lead comprising an inner pad and an outer pad connected by a connection member, wherein a region of said inner pad and a region of said outer pad are separated by a channel extending through a width of said lead.

27. The lead frame of claim 26, wherein said connection member has a thickness that is approximately half a thickness of said lead.

28. The lead frame of claim 26, wherein said connection member is integral with said inner pad.

29. The lead frame of claim 28, wherein said connection member is integral with said outer pad.

30. The lead frame of claim 26, wherein said lead is one of a plurality of inwardly projecting leads, each lead comprising an inner pad, and said inner pad of at least one of said leads projects further inward than another of said inner pads of said leads.

31. The lead frame of claim 26, wherein said lead is one of a plurality of leads, each lead comprising an inner pad and an outer pad, and a distance between adjacent inner pads is less than a distance between adjacent outer pads.

32. The lead frame of claim 26, wherein said lead is one of a plurality of leads, each lead comprising an inner pad, and a width of at least one inner pad is less than a width of another inner pad.

33. The lead frame of claim 26, wherein a thickness of said inner pad is substantially equal to a thickness of said outer pad.

34. The lead frame of claim 26, wherein said connection member has a thickness that is approximately half a thickness of said lead.

35. The integrated circuit package of claim 3:

wherein said connection member is integral with said inner pad and said outer pad;

wherein said connection member has a thickness that is approximately half a thickness of said lead;

wherein said encapsulant further encapsulates substantially all of said connection member; and

wherein a thickness of said inner pad is substantially equal to a thickness of said outer pad.

36. The integrated circuit package of claim 35, wherein said lead is one of a plurality of inward projecting leads, each lead comprising an inner pad, and said inner pad of at least one of said leads projects further inward than another of said inner pads of said leads.

37. The integrated circuit package of claim 35, wherein said lead is one of a plurality of leads, each lead comprising an inner pad and an outer pad, and a distance between adjacent inner pads is less than a distance between adjacent outer pads.

38. The integrated circuit package of claim 35, wherein said lead is one of a plurality of leads, each lead comprising an inner pad, and a width of at least one inner pad is less than a width of another inner pad.

39. The integrated circuit package of claim 35, further comprising a second semiconductor die electrically coupled with a second inner pad of a second lead.

40. A lead frame, comprising:

a lead comprising a means for connecting an inner pad and an outer pad of said lead, wherein a region of said inner pad and a region of said outer pad are separated by a channel extending through a width of said lead.

41. An integrated circuit package comprising the lead frame of claim 40.

42. The integrated circuit package of claim 41, further comprising:

a semiconductor die electrically coupled with said inner pad of said lead; and

a wire attached between said semiconductor die and said inner pad, wherein a length of said wire is about 150 mils or less.

43. The integrated circuit package of claim 41, wherein said lead is one of a plurality of inwardly projecting leads, each lead comprising an inner pad, and said inner pad of at least one of said leads projects further inward than another of said inner pads of said leads.

44. The integrated circuit package of claim 41, wherein said lead is one of a plurality of leads, each lead comprising an inner pad and an outer pad, and a distance between adjacent inner pads is less than a distance between adjacent outer pads.

45. The integrated circuit package of claim 41, wherein said lead is one of a plurality of leads, each lead comprising an inner pad, and a width of at least one inner pad is less than a width of another inner pad.

46. The integrated circuit package of claim 41, further comprising an encapsulant material encapsulating at least a portion of said lead frame.

47. The integrated circuit package of claim 46, wherein a portion of said outer pad is exposed.

48. The integrated circuit package of claim 46, further comprising a semiconductor die electrically coupled with said inner pad of said lead.

49. The integrated circuit package of claim 1, wherein a portion of said outer pad is exposed.

50. The integrated circuit package of claim 14, wherein a portion of said outer pad is exposed.

51. The integrated circuit package of claim 46, wherein said encapsulant further encapsulates substantially all of said connection member.

52. The integrated circuit package of claim 41, wherein said lead is one of a plurality of leads, each lead comprising an inner pad, and wherein said package further comprises a plurality of semiconductor dies electrically coupled with said inner pads.

53. The integrated circuit package of claim 41, wherein a thickness of said inner pad is substantially equal to a thickness of said outer pad.

54. The integrated circuit package of claim 1, wherein said encapsulant material comprises an epoxy-based material.

55. The integrated circuit package of claim 7, further comprising a die attachment pad configured to accommodate a contour defined by said inner pads of said leads.

56. The integrated circuit package of claim 1:

wherein said lead is one of a plurality of inwardly projecting leads, each lead comprising an inner pad, and

wherein said package further comprises a die attachment pad configured to accommodate a contour defined by said inner pads of said leads.

57. The integrated circuit package of claim 41,

wherein said lead is one of a plurality of inwardly projecting leads, each lead comprising an inner pad, and

wherein said package further comprises a die attachment pad configured to accommodate a contour defined by said inner pads of said leads.

58. The lead frame of claim 26, wherein said lead is one of a plurality of leads, each lead comprising a connection member, and wherein at least two of said connection members have different lengths.

59. The integrated circuit package of claim 1,

wherein said lead is one of a plurality of leads, each lead comprising a connection member, and

wherein at least two of said connection members have different lengths.

60. The integrated circuit package of claim 1, further comprising a die attachment pad, wherein at least a portion of said die attachment pad is exposed.

61. The integrated circuit package of claim 60, wherein said die attachment pad and said semiconductor die are attached by a soft solder.

62. The integrated circuit package of claim 60, wherein at least a portion of said outer pad is exposed.

63. The integrated circuit package of claim 62, wherein at least a portion of said inner pad is exposed.

64. The integrated circuit package of claim 41, further comprising a die attachment pad, wherein at least a portion of said die attachment pad is exposed.

65. The integrated circuit package of claim 64, wherein at least a portion of said outer pad is exposed.

66. The integrated circuit package of claim 65, wherein at least a portion of said inner pad is exposed.

67. The lead frame of claim 26, wherein said lead frame is made of an electrically conductive material.

68. The lead frame of claim 67, wherein said electrically conductive material comprises copper.

69. The lead frame of claim 67, wherein said electrically conductive material comprises a compound.

70. The lead frame of claim 26, wherein a width of said outer pad is about 0.230 mm.

71. The lead frame of claim 70, wherein a length of said outer paid is about 0.550 mm.

72. The lead frame of claim 71, wherein said lead comprises one of a plurality of leads, each lead comprising an outer pad, wherein a pitch of adjacent outer pads is about 0.500 mm.

73. The integrated circuit package of claim 1, wherein said lead frame is pre-plated with palladium.

74. The integrated circuit package of claim 1, wherein at least a portion of an upper and a lower surface of said lead are plated with solder.

75. The integrated circuit package of claim 1, wherein at least a portion of an upper and a lower surface of said lead are plated with tin.

76. The integrated circuit package of claim 1, wherein said lead is one of a plurality of leads, each lead comprising an inner pad and an outer pad, wherein said outer pads are arranged in a generally angular configuration.

77. The integrated circuit package of claim 76, wherein said inner pads are arranged in a generally angular configuration.

78. The integrated circuit package of claim 1, wherein said lead is one of a plurality of leads, each lead comprising an inner pad and an outer pad, wherein said inner pads are spaced more closely together than said outer pads.

79. The lead frame of claim 26, wherein said lead is one of a plurality of leads, each lead comprising an inner pad and an outer pad, wherein said inner pads are spaced more closely together than said outer pads.

80. The integrated circuit package of claim 1, wherein said inner pad has a

planform area smaller than a planform area of said outer pad.

81. The lead frame of claim 26, wherein said inner pad has a platform area smaller than a planform area of said outer pad.

82. The integrated circuit package of claim 1, wherein said semiconductor die is one of a plurality of semiconductor dies.

83. The integrated circuit package of claim 82, further comprising a die attachment pad attached to said plurality of semiconductor dies.

84. The method of claim 18, wherein said encapsulating comprises employing a liquid encapsulating process.

85. The method of clam 18, wherein said encapsulating comprises employing a transfer molding process.

86. The method of claim 15, wherein said lead frames are substantially identical.

87. The method of claim 15, wherein said matrix of lead frames is one of a plurality of matrices of lead frames formed in a frame area of a strip.

88. The method of claim 87, wherein a periphery of said strip comprises an assembly feature for use in automated assembly equipment.

89. The method of claim 88, wherein said assembly feature comprises an alignment target.

90. The method of claim 88, wherein said assembly feature comprises a tooling hole.

91. A method, comprising:

creating a lead from a sheet; and

forming a channel extending through a width of said lead to create an inner pad, an outer pad and a connection member in said lead.

92. The method of claim 91, wherein said creating comprises stamping.

93. The method of claim 91, wherein said sheet comprises a metal.

94. The method of claim 93, wherein said metal comprises copper.

95. The method of claim 91, wherein said creating further comprises creating a plurality of leads in a generally annular configuration, each lead comprising an inner pad, an outer pad and a connection member.

96. The method of claim 95, wherein said creating further comprises creating a die attachment pad.

97. The method of claim 96, further comprising mounting a semiconductor die on said die attachment pad.

98. The method of claim 97, further comprising mounting a second semiconductor die on said die attachment pad.

99. The method of claim 91, wherein said forming comprises etching said channel into said lead.

100. The method of claim 99, wherein said etching comprises a chemical etching process.

101. The method of claim 99, wherein said etching comprises etching said channel to a thickness of approximately half a thickness of said lead.

102. The method of claim 100, wherein said chemical etching process comprises masking a portion of said lead.

103. The method of claim 91, further comprising electrically coupling a

semiconductor die with said inner pad.

104. The method of claim 103, further comprising attaching a solder member to said outer pad.

105. The method of claim 103, wherein said electrically coupling comprises attaching a wire between said semiconductor die and said inner pad by a thermo-sonic bonding process; and

wherein said bonding process comprises attaching said wire to a top side of said inner pad while a support contacts a bottom side of said inner pad and bottom side of said outer pad.

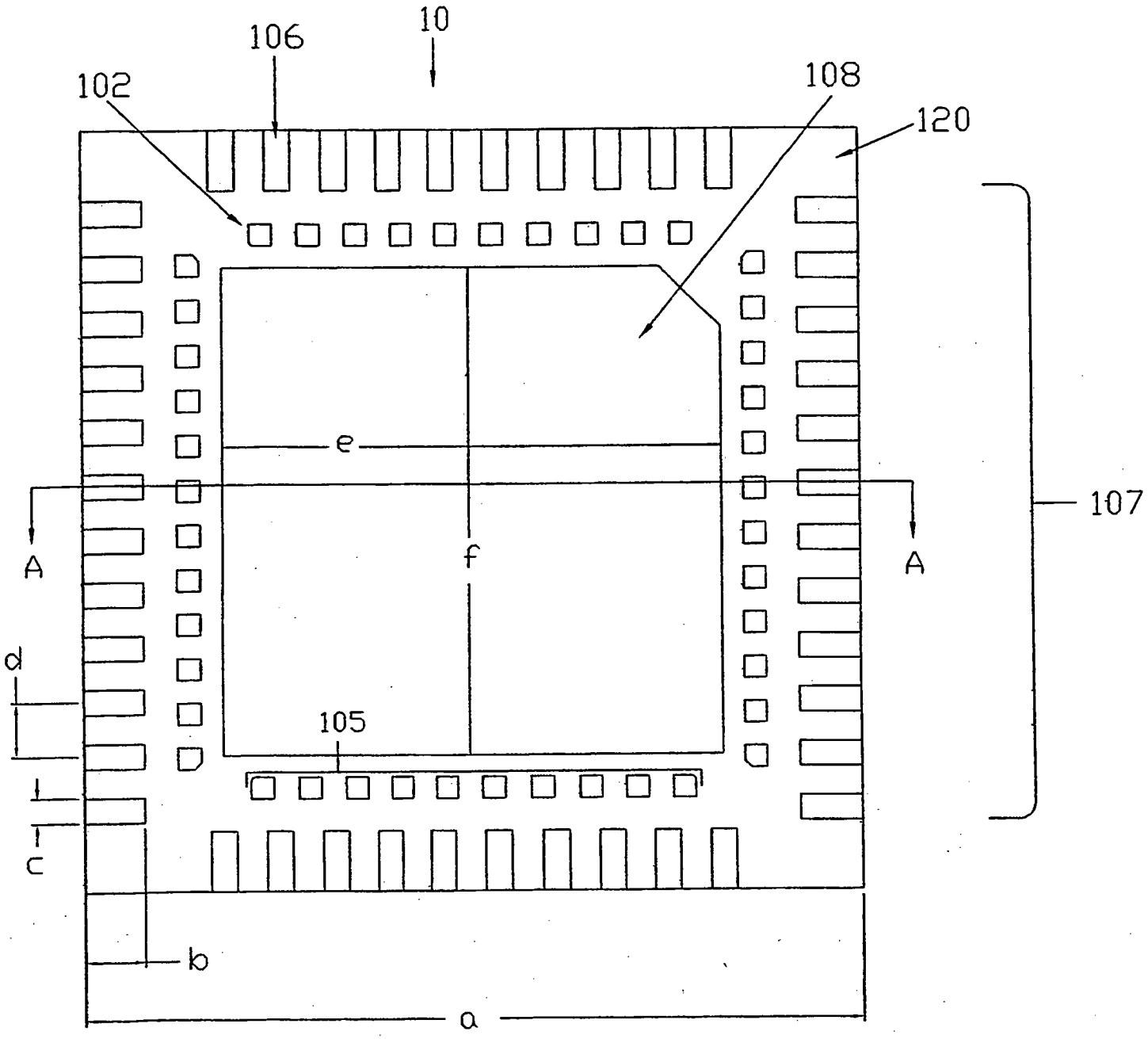



FIG.1

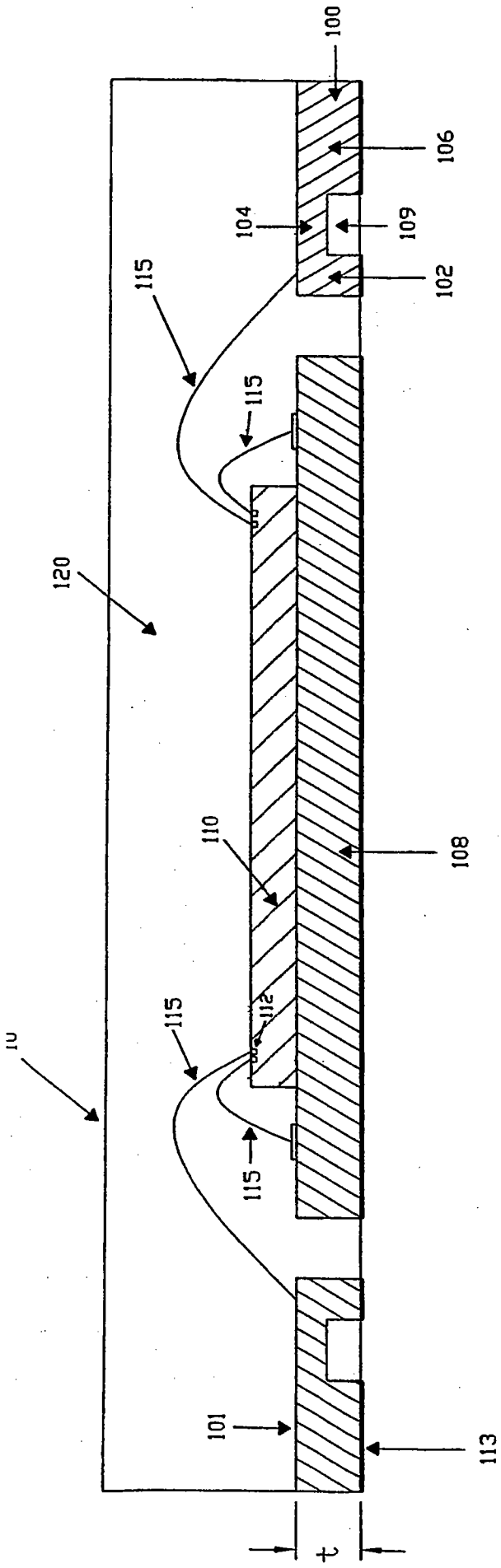



FIG.2

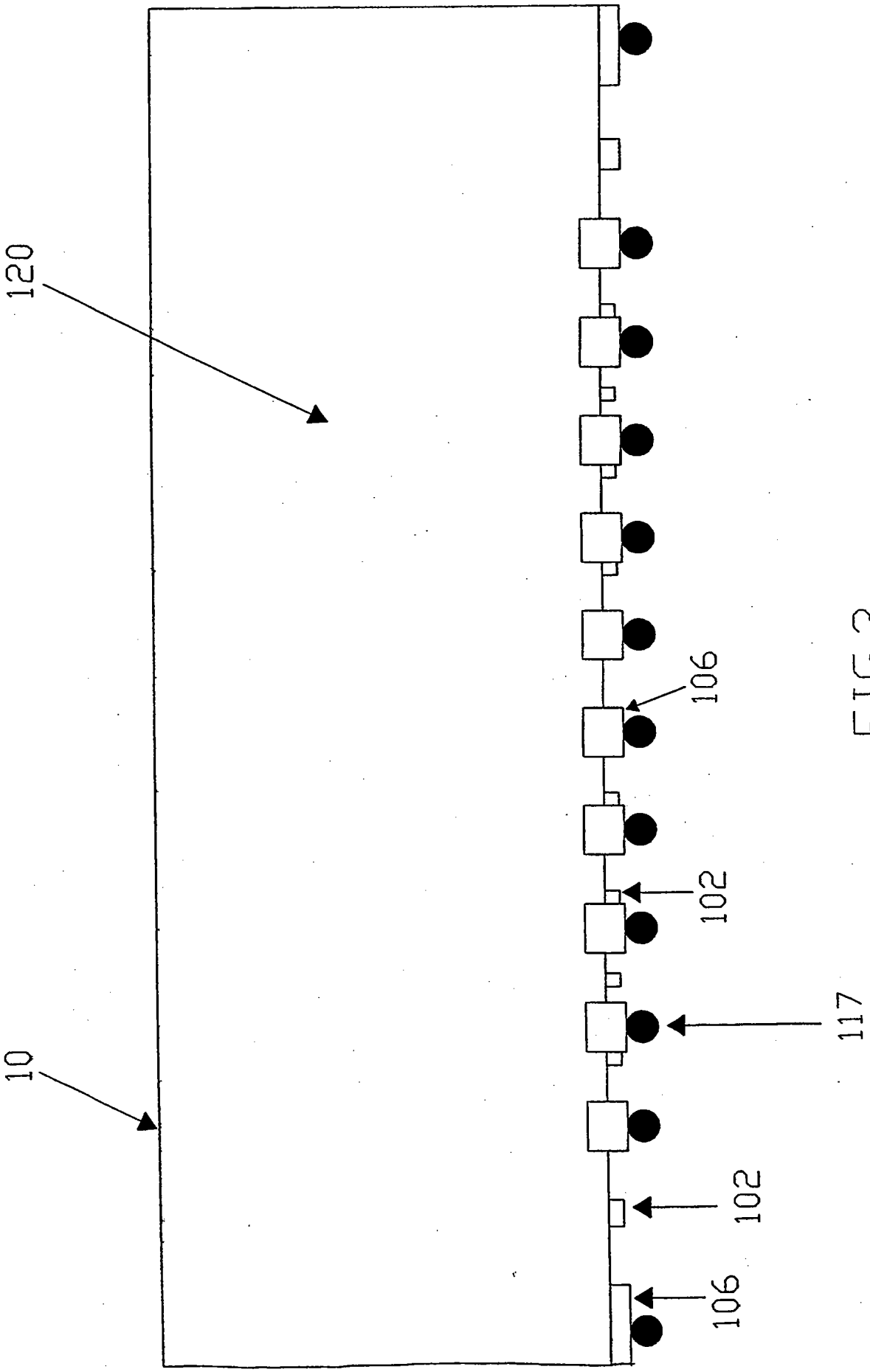



FIG.3

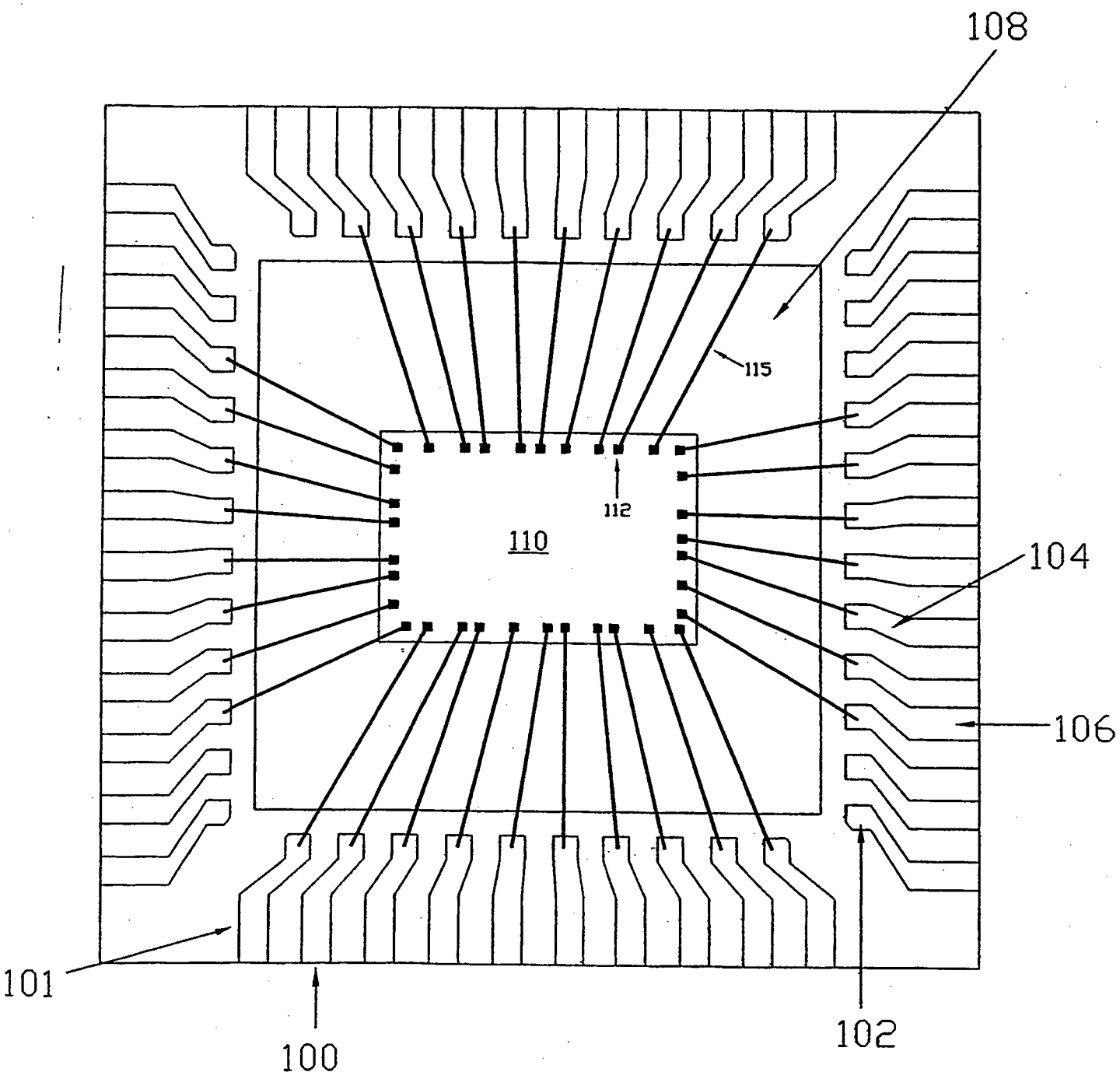



FIG.4

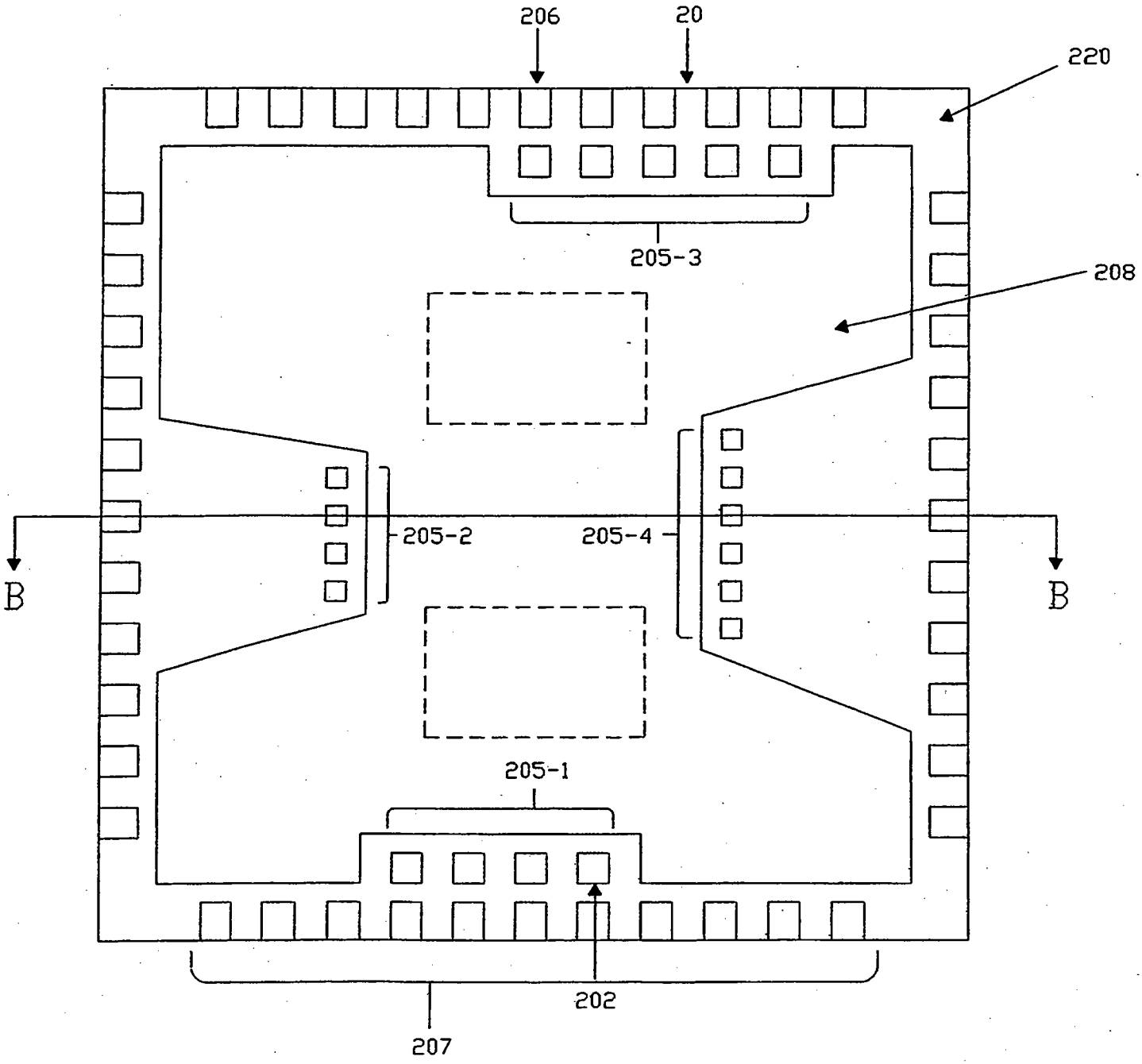



FIG.5

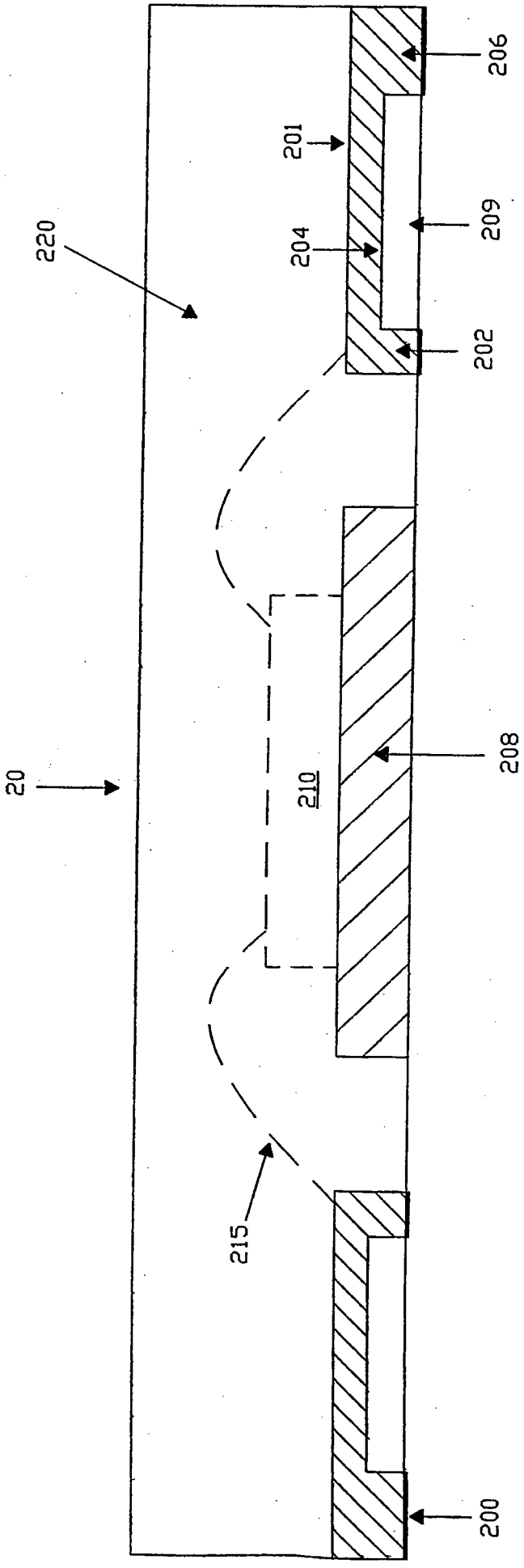



FIG.6

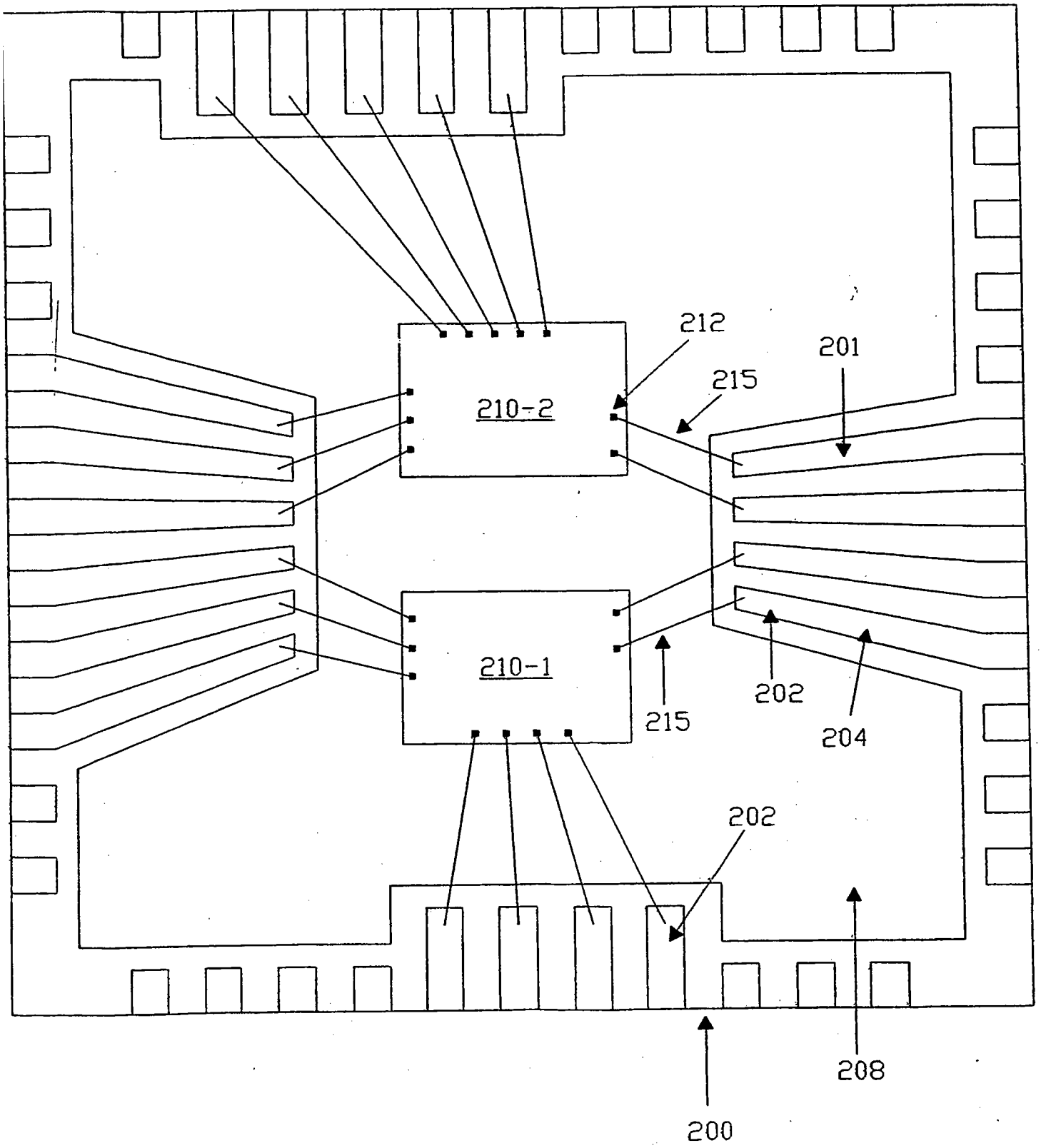



FIG.7

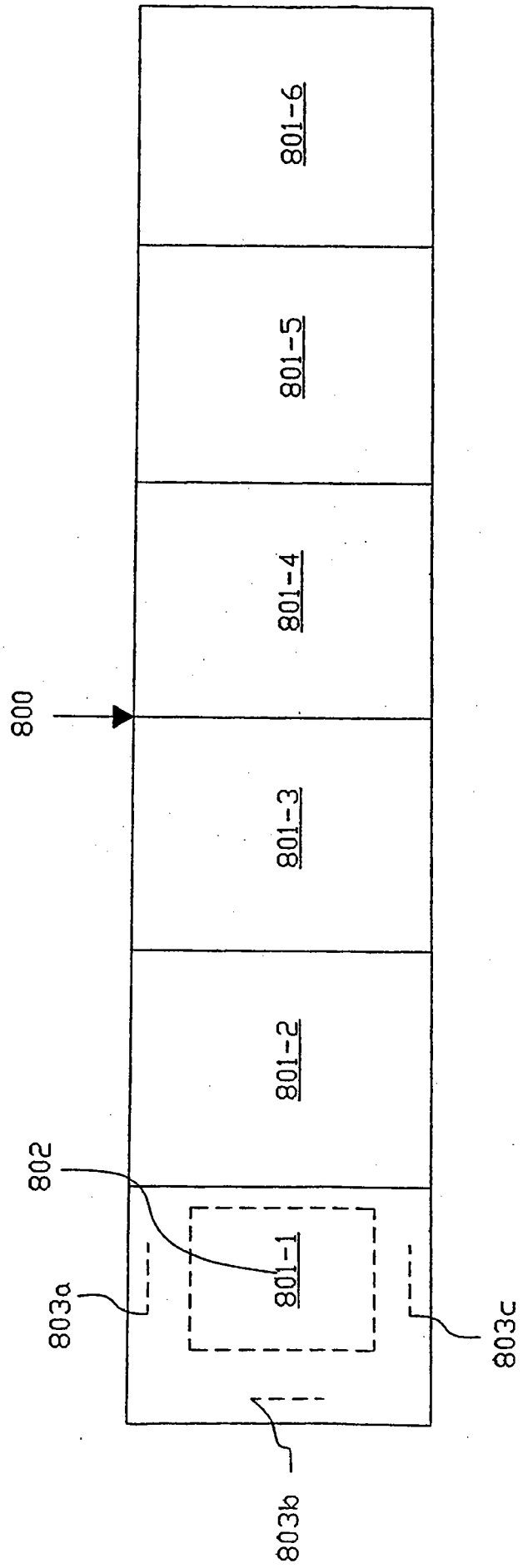



FIG.8

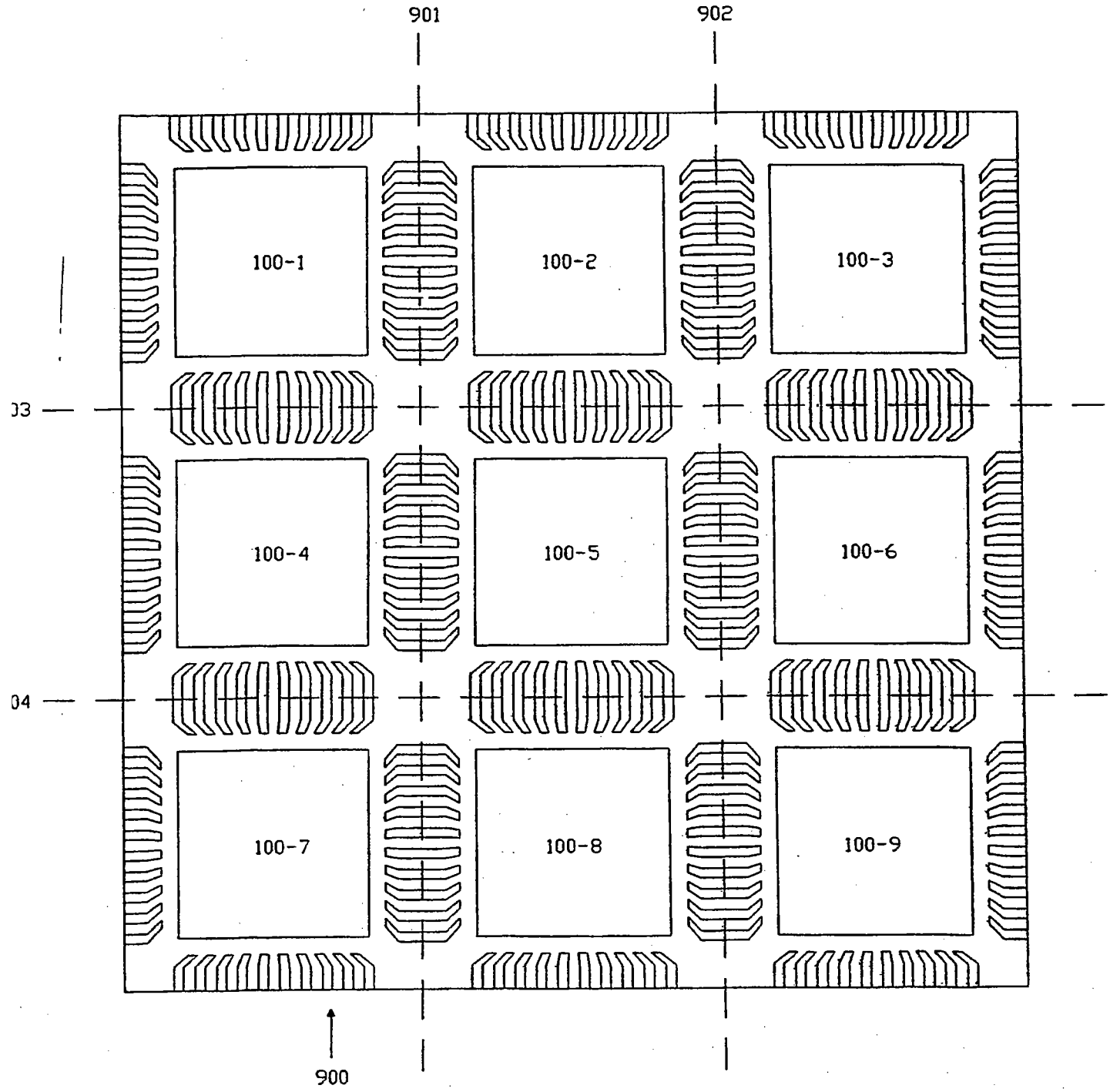
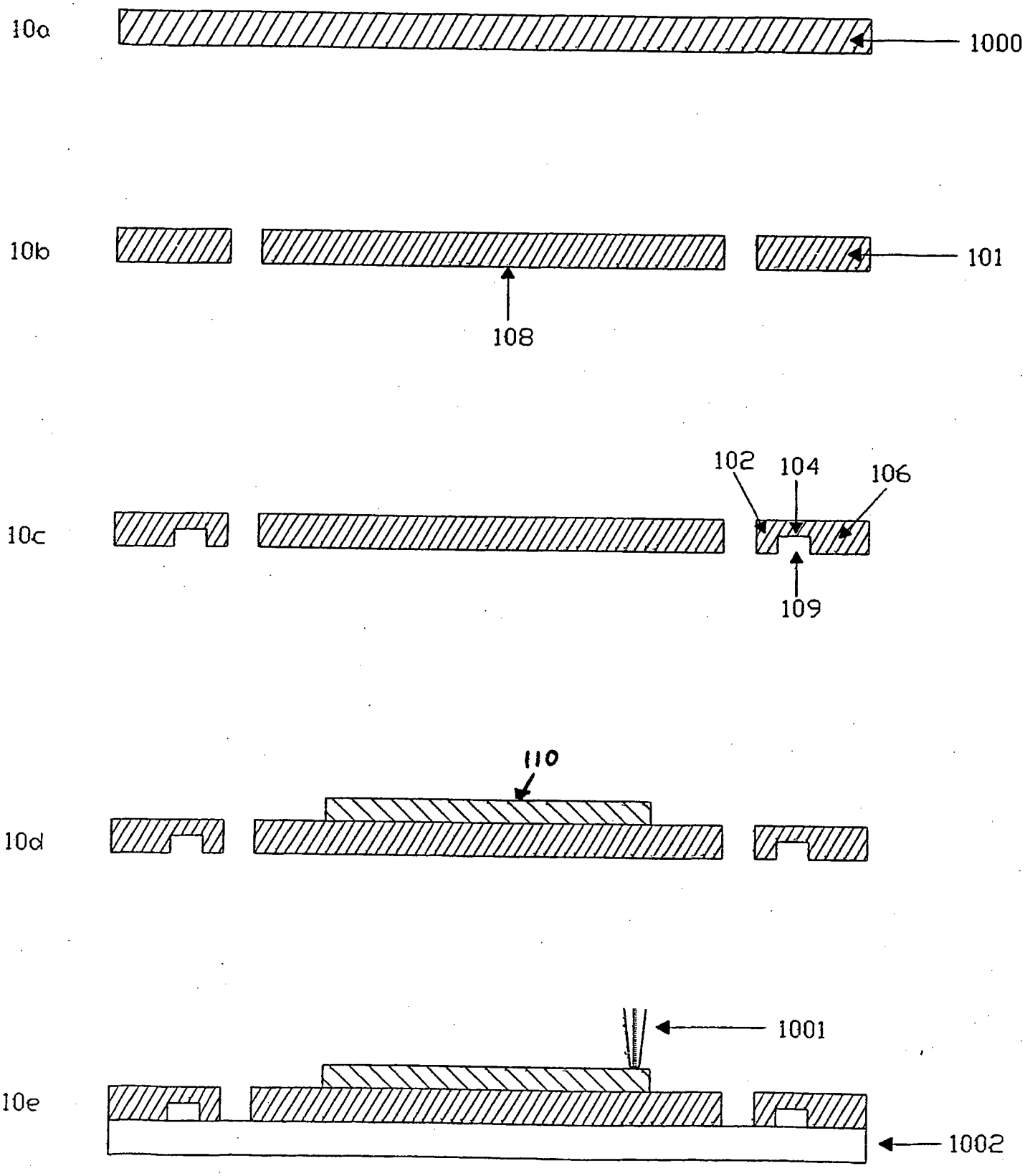



FIG.9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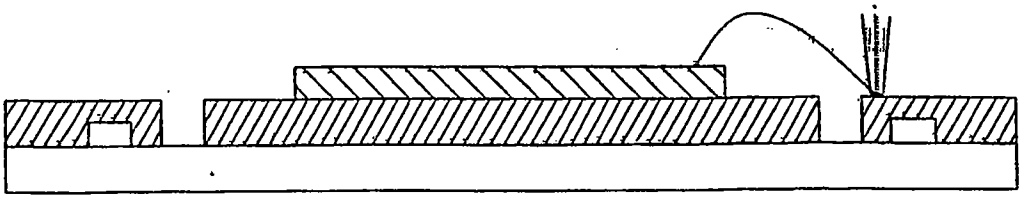

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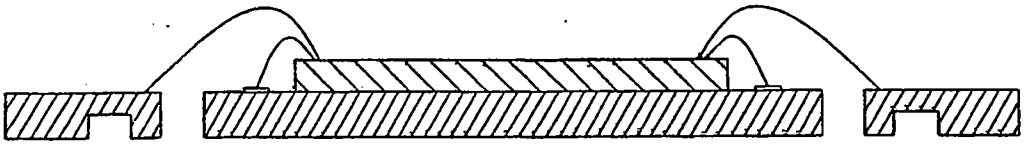

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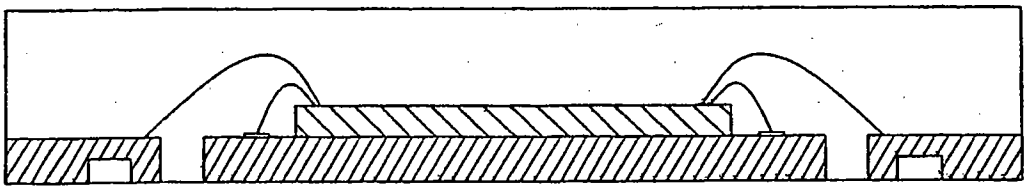

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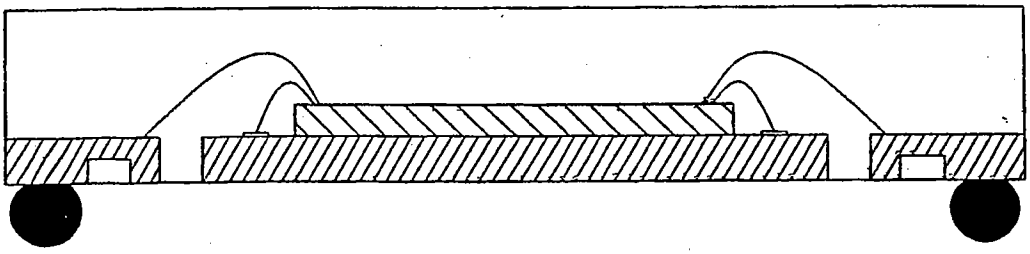

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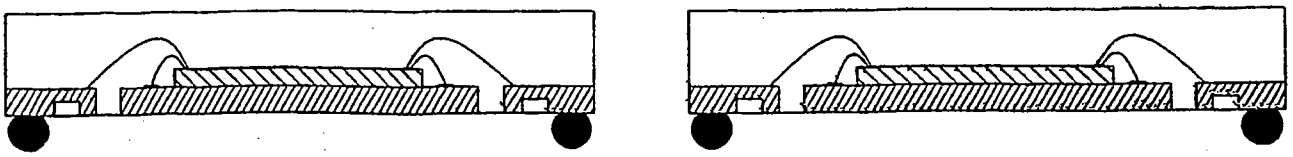

SINGULATION

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/US03/20008

**A. CLASSIFICATION OF SUBJECT MATTER**

IPC(7) :H01L 23/495, 23/48, 23/52, 23/28, 29/40
US Cl. : 257/666, 672, 674, 676, 786, 787, 782, 784
According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/666, 672, 674, 676, 786, 787, 782, 784

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

None

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

None

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | US 6,143,981 A (GLENN) 07 NOVEMBER 2000 (07/11/2000), FIG. 8. | 40, 41, 91, 93 |
| A | US 5,796,589 A (BARROW) 18 AUGUST 1998 (18/08/1998), FIG. 2. | 1-105 |
| X | US 6,242,281 B1 A (McLELLAN ET AL.) 05 JUNE 2001 (05/06/2001), FIG. 4A. | 1, 2, 18, 40, 41 |
| A | US 6,011,694 A (HIRAKAWA) 04 JANUARY 2000 (04//01/2000), FIG. 7. | 1-105 |

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

| | | | |
|---|---|---|---|
| * | Special categories of cited documents | "T" | later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention |
| "A" | document defining the general state of the art which is not considered to be of particular relevance | "X" | document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone |
| "E" | earlier document published on or after the international filing date | "Y" | document of particular relevance, the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art |
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| "O" | document referring to an oral disclosure, use, exhibition or other means | | |
| "P" | document published prior to the international filing date but later than the priority date claimed | | |

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| Date of the actual completion of the international search<br>05 SEPTEMBER 2003 | Date of mailing of the international search report<br>03 NOV 2003 |
| Name and mailing address of the ISA/US<br>Commissioner of Patents and Trademarks<br>Box PCT<br>Washington, D.C. 20231<br>Facsimile No. (703) 305-3230 | Authorized officer<br>JASMINE J B CLARK<br>Telephone No. (703) 308-4857 |

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